Double Data Rate Synchronized Random Access Memory

And other phrases you can say to make you light headed

Dominick Christensen

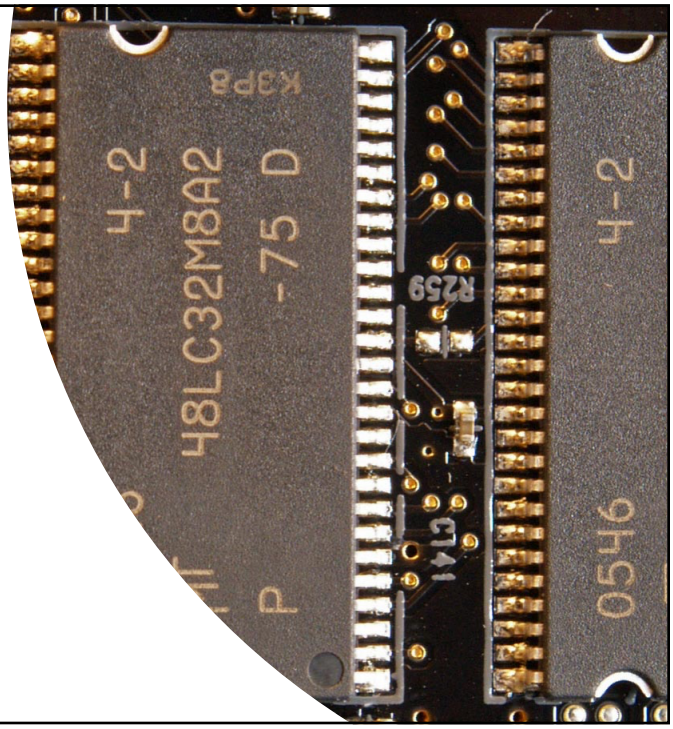
DRAM

- Robert Dennard had an idea to store information in the positive/negative charge of a capacitor.
- This charge was short lived but Dennard devised a way to use a FET to read and refresh the charge on a capacitor.
- This dynamic RAM largely replaced the bulky and power hungry RAM of before and remain in use for the next twenty years.

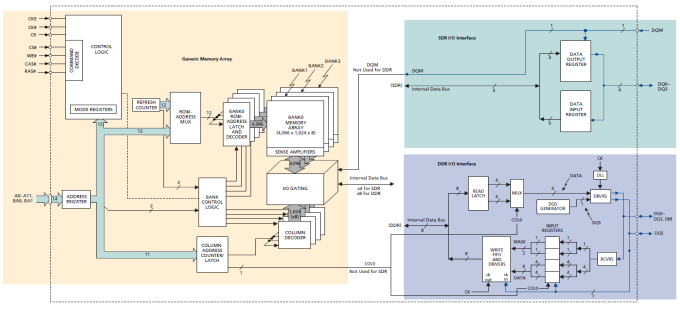
Pictured: Not Robert Dennard

SDRAM

- First commercial SDRAM unit made available in 1992
- Synchronizing the DRAM to the clock allowed for commands to the DRAM unit to be pipelined, improving performance.
- Memory is divided into independent “banks”, allowing greater concurrency and higher data transfer rates than asynchronous DRAM



DDR SDRAM: The Next Generations



Ones and Twos

DDR1

- Reads off the rising and falling clock edge
- Strict control over timing of electrical and clock signals
- 2n Prefetch Technology Allows for "quick and easy" access to multiple data words on a common physical row in memory

DDR2

- Prefetch increased to 4n
- Bandwidth and Bus Clock Rate doubles
- Voltage requirements reduced

Threes and Fours

DDR3

- Operation speed double of DDR2 and quadruple DDR1
- Prefetch increases to 8n
- Reduced voltage requirements and enhanced low power features

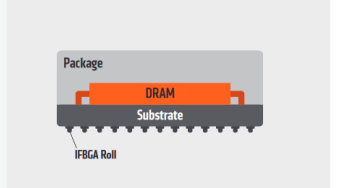
DDR4 (The Current Generation)

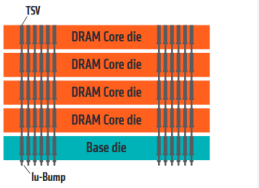
- No prefetch increase, but more read/write commands per second
- New features such as Data Bus Inversion, Cyclic Redundancy Check and CA parity improve signal integrity and stability of data transmission
- Further divides DRAM banks into 2-4 selectable bank groups

What's next?

- DDR5
  - Increased Bank Groups, Burst Lengths for improved density and data bus efficiency
  - 16n Prefetch
  - Up to 64GB memory density
- High Bandwidth Memory
  - Vertically stacked memory chips
  - Shortened information commute
  - Massive Space Savings

HBM vs GDDR5:
Compare side by side





GDDR5	Per Package	HBM
32-bit	Bus Width	1024-bit
Up to 1750MHz (7GBps)	Clock Speed	Up to 500MHz (1GBps)
Up to 28GB/s per chip	Bandwidth	>100GB/s per stack
1.5V	Voltage	1.3V

Questions?

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Sources

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